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(h) forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film.

REMARKS

Favorable reconsideration of this application, as amended, is respectfully requested.

A new title has been provided as required.

The rejection of Claims 1-16 under 35 U.S.C. § 103(a) is addressed in these remarks. The Examiner is authorized to cancel non-elected Claims 17-19 in order to pass this application to issue.

Independent Claims 1, 6, 11, and 14 have been amended to clarify the manner in which Applicants' invention distinguishes patentably from the prior art, and in particular, Tsai (U.S. Patent No. 5,763,306) relied upon in the rejection under 35 U.S.C. § 103(a). Dependent Claims 2, 4, 5, and 10 have also been amended, but the amendment of these claims is not required to overcome the rejection, because, as will appear hereinafter, their base claims are patentable. Claims 3, 7-9, and 13 have been cancelled as no longer necessary.

A significant, and patentable difference between Applicants' invention and Tsai is that in Applicants' invention, a rugged surface silicon film (also referred to as HSG silicon) is formed on a silicon film only on an inner surface of a trench, while in the Tsai patent, a rugged surface silicon film is formed on a silicon film that extends well beyond the inner surface of a trench.

As shown in Fig. 7, of Applicants' drawings, the rugged surface silicon film 43b is formed on a silicon film 43a only on an inner surface of a trench. As shown in Figs. 8A and 8B of the Tsai patent, a rugged surface silicon film 20 is formed on a silicon film 19 that extends well beyond a trench. With the method disclosed by Tsai, defect density tends to be increased and manufacturing yield tends to deteriorate.

Independent Claims 1, 6, 11, and 14 clearly recite that a silicon film on an insulating film and in a trench is removed to leave the silicon film only on an inner surface of the trench and that a rugged surface silicon film is formed on the silicon film on the inner surface of the trench, clearly distinguishing patentably from Tsai.

Independent Claims 6 and 11 also recite depositing or forming an insulating film at a temperature range of 450°C

to 700°C. This temperature range is high enough to avoid the need for subsequent heat treatment to remove moisture in the insulating film. Growth of a rugged surface silicon is hindered by the effect of moisture in the insulating film (see the sentence bridging pages 2-3 of Applicants' specification), but high temperature heat treatment to remove the moisture in the insulating film is deleterious to the properties of MISFETs (see page 3 and page 4, lines 1-8 of Applicants' specification).

As recognized in the rejection, Tsai teaches temperatures as high as 800°C to 850°C. Such high temperatures can cause deterioration of the properties of a semiconductor device, particularly where Boron leakage is of concern (see the paragraph bridging pages 3-4 of Applicants' specification). Such concern is important in the manufacture of a semiconductor integrated circuit that includes both a memory cell and a logic circuit, as recited in dependent Claims 4 and 10 based on Claims 1 and 6, respectively, which recite the temperature range of 450°C-700°C This temperature range makes it possible to form a silicon oxide film 41 having low moisture and impurity contents (see page 16, lines 17-24 of Applicants' specification). Heat treatment at a temperature of about

600°C to polycrystallize the amorphous silicon film 43a to cause the growth of silicon grains 43b does not have the deleterious effects of high temperature heat treatments (see page 18, lines 4-22; page 19, lines 3-25; and page 20, lines 4-21 of Applicants' specification).

For the foregoing reasons, it is respectfully submitted that all of Claims 1-16 should be allowed and that this application should be passed to issue.

A marked-up copy of the amended claims is attached.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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Marked-up copy of Claims - 10/083,416

1. (Amended) A manufacturing method of a semiconductor integrated circuit device comprising a memory cell formed of a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

(a) forming said MISFET on the main surface of said semiconductor substrate;

(b) forming an insulating film above said MISFET by the plasma CVD method at a temperature of 450°C to 700°C;

(c) forming a trench by etching said insulating film;

[and]

(d) depositing a silicon film on said insulating film and in said trench, and removing the silicon film on said insulating film to [form a lower electrode of said capacitor on the inner wall of the trench] leave the silicon film only on an inner surface of said trench;

(e) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of said capacitor on the inner wall of the trench; and

(f) forming a dielectric film on said rugged surface silicon film and on said insulating film and forming a plate electrode on said dielectric film.

2. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said rugged surface silicon film is formed by crystal grains which are grown from crystal nucleuses of silicon [are formed on a surface of the silicon film of said step (d)] deposited on said silicon film.

4. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said semiconductor integrated circuit device has [an] a first area in which said memory cell is formed and [an] a second area in which a logic circuit is formed, and said manufacturing method of a semiconductor integrated circuit device comprises, before said step (b), the step of:

(e) forming, in said second area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n

channel MISFET and said p channel MISFET comprising a gate electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

5. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said plasma CVD method is [the CVD method using] a high-density plasma CVD.

6. (Amended) A manufacturing method of a semiconductor integrated circuit device comprising a memory cell including [formed of] a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

(a) forming said MISFET on the main surface of said semiconductor substrate;

(b) depositing a first insulating film above said MISFET at a [predetermined] first temperature;

(c) depositing a second insulating film on said first insulating film at a second temperature between 450°C and 700°C that is higher than said [predetermined] first temperature;

(d) forming a trench by etching said first and second insulating films; [and]

(e) depositing a silicon film on said second insulating film and in said trench, and removing the silicon film on said second insulating film to [form a lower electrode of said capacitor on the inner wall of the trench] leave the silicon film only on an inner surface of said trench;

(f) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of said capacitor on the inner wall of the trench; and

(g) forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film.

10. (Amended) The manufacturing method of a semiconductor integrated circuit device according to claim 6,

wherein said semiconductor integrated circuit device has a first [an] area in which said memory cell is formed and [an] a second area in which a logic circuit is formed, and said manufacturing method of a semiconductor integrated

circuit device comprises, before said step (b), the step of:

[(f)] (h) forming, in said second area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n channel MISFET and said p channel MISFET comprising a gate electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

11. (Amended) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate; [and]

(b) forming an insulating film containing impurity above said MISFET by [the] a high density plasma CVD method at a temperature of 450°C to 700°C;

(c) forming a trench by etching said insulating film;

(d) depositing a silicon film on said insulating film and in said trench, and removing the silicon film on said insulating film to leave the silicon film only on an inner surface of said trench;

(e) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of a capacitor on the inner wall of the trench; and

(f) forming a dielectric film on said rugged surface silicon film and on said insulating film and forming a plate electrode on said dielectric film.

14. (Amended) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate;

(b) depositing a first insulating film above said MISFET at a [predetermined] first temperature;

(c) planarizing a surface of said first insulating film; [and]

(d) forming a second insulating film containing impurity on said first insulating film at a second temperature higher than said [predetermined] first temperature;

(e) forming a trench by etching said first and second insulating films;

(f) depositing a silicon film on said second insulating film and in said trench, and removing the silicon film on said second insulating film to leave the silicon film only on an inner surface of said trench;

(g) forming a rugged surface silicon film on said silicon film on said inner surface of said trench to form a lower electrode of a capacitor on the inner wall of the trench; and

(h) forming a dielectric film on said rugged surface silicon film and on said second insulating film and forming a plate electrode on said dielectric film.